AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A memory cell comprising:

two electrodes;

a polymeric body, between the electrodes, having a plurality of roughness formations on a surface thereof, the roughness formations having a height, the polymeric body having a property capable of maintaining a charge after a voltage is applied across the electrodes; and

~~an~~ a first interface material having a first portion and a second ~~portions~~interface material having a second portion, the first portion being between one of the electrodes and the surface of the polymeric body and having a first thickness that is greater than the height of the roughness formations, the second portion being between the other electrode and an opposing surface of the polymeric body and having a second thickness that is less than the first thickness.

2. (Original) The memory cell of claim 1, wherein the polymeric body maintains a second charge after a second voltage is applied across the electrodes.

3. (Currently Amended) The memory cell of claim 2, wherein the first portion of the first interface material completely separates ~~the at least~~ one electrode and the polymeric body.

4. (Currently Amended) The memory cell of claim 3, wherein the thickness of the first portion of the first interface material is at least 150 angstroms.

5. (Original) The memory cell of claim 4, wherein the electrodes are metal.

6. (Original) The memory cell of claim 5, wherein the electrodes are made of at least one of titanium nitride, titanium, and aluminum.

7. (Original) The memory cell of claim 6, wherein the polymeric body is ferroelectric.

8. (Original) The memory cell of claim 7, wherein the polymeric body includes fluorine.

9. (Original) The memory cell of claim 8, wherein the height of the roughness formation is between 600 and 1000 angstroms.

10. (Currently Amended) The memory cell of claim 6, wherein the first portion of the first interface material is titanium oxide.

11. (Previously Presented) A semiconductor device comprising;

a substrate;

a first layer, on the substrate, having a plurality of first conductive lines therein;

a second layer, on the first layer, having a plurality of lower interface sections, each lower interface section being over at least a portion of at least one of the first conductive lines, each lower interface section having a first thickness;

a third layer, on the second layer, having a plurality of polymeric sections, each polymeric section being over at least a portion of at least one of the lower interface sections, the polymeric sections having a plurality of roughness formations on a surface thereof, the roughness formations having a height;

a fourth layer, on the third layer, having a plurality of interface upper sections, each upper interface section being adjacent to at least one of the polymeric sections, each upper interface section having a second thickness that is greater than the height of the roughness formations and the first thickness; and

a fifth layer, on the fourth layer, having a plurality of second conductive lines therein, each second conductive line extending over at least one first conductive line, at least one polymeric section, and at least one upper and lower interface section to form a plurality of memory cells such that a voltage applied across one of the first conductive lines and one of the second conductive lines changes a charge of the polymeric section from a first value to a second value.

12. (Previously Presented) The semiconductor device of claim 11, wherein the thickness of each interface upper section is at least 150 angstroms.

13. (Original) The semiconductor device of claim 12, wherein the substrate is silicon and has mircoelectronic circuitry formed therein.

14. (Original) The semiconductor device of claim 13, further comprising an insulating layer between the substrate and the first layer.

15. (Original) The semiconductor device of claim 14, wherein the insulating layer is silicon oxide.

16. (Original) The semiconductor device of claim 15, wherein the first and second conductive lines are made of at least one of titanium nitride, titanium, and aluminum.

17. (Original) The semiconductor device of claim 16, wherein the polymeric sections are ferroelectric.

18. (Original) The semiconductor device of claim 17, wherein the height of the roughness formations is between 600 and 1000 angstroms.

19. (Previously Presented) The semiconductor device of claim 18, wherein each interface upper section is made of titanium oxide.

20. (Original) The semiconductor device of claim 19, wherein said layers are stacked vertically.

21-30. (Canceled)